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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,036	09/18/2006	Teruo Amoh	20239/0204318-US0	3301

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/599,036	AMOH ET AL.	
	Examiner	Art Unit	
	Alexander Belousov	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 0200* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/18/2006 & 05/08/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 09/18/2006 & 05/08/2007. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 10 & 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim limitations of "a semiconductor light-emitting device wherein a semiconductor light-emitting element is mounted in a semiconductor light-emitting element mounting member according to claim 1", as recited in claim 10 are indefinite because "a semiconductor light-emitting device" does not further limit the structure of "element mounting member".

The claim limitations of "A semiconductor light-emitting device", as recited in claim 11 are indefinite because "a semiconductor light-emitting device" does not further limit the structure of "element mounting member".

The claim limitations of "output is at least 1 W", as recited in claim 11, are unclear as to what does "output" refers to.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-4, 6, 9 & 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over (JP-2003-209286) by Kitano in view of Silicon Processing for VLSI Era Volume 1 by Wolf et al.

Regarding claim 1, Kitano discloses in FIG. 3 and related text (machine translation of the publication has been included) a semiconductor light-emitting element mounting member comprising: a substrate (111); and a metal film (107) formed on a surface of said substrate, formed from Ag, Al, or an alloy containing said metals, and functioning as an electrode layer for mounting at least one of a semiconductor light-emitting element (100) and a reflective layer for reflecting light from a semiconductor light-emitting element.

Kitano does not disclose the thickness of the metal film is 0.5-3 .mu.m and crystal grains of said metal or alloy forming said metal film have a particle diameter along a surface plane of said metal film is no more than 0.5 .mu.m and said surface of said metal film has a center-line average roughness Ra of no more than 0.1 .mu.m.

Wolf teaches the thickness of the metal film is 0.5-3 .mu.m (page 435; "thickness range of 500-1500 nm") and crystal grains of said metal or alloy forming said metal film have a particle diameter along a surface plane of said metal film is no more than 0.5 .mu.m and said

surface of said metal film has a center-line average roughness Ra of no more than 0.1 .mu.m (pages 106-107 describe the vapor deposition process; bottom of page 106: smaller grains are result of lower substrate temperature; top of page 107: smaller grains are result of higher deposition rates; these are the two methods stated by applicant in his disclosure for achieving his particle diameter and roughness specs; hence, these results are **inherent** in the application of Wolf's teaching by applicant's own disclosure; NOTE: applicant states one more factor which **may** affect particle diameter and roughness specs: roughness of the substrate; however, applicant discloses that this is not a strict requirement (page 16: "**may** not be possible")).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Kitano with the thickness of the metal film is 0.5-3 .mu.m and crystal grains of said metal or alloy forming said metal film have a particle diameter along a surface plane of said metal film is no more than 0.5 .mu.m and said surface of said metal film has a center-line average roughness Ra of no more than 0.1 .mu.m as taught by Wolf, in order to simplify the manufacturing process, by using conventional & well-known materials (page 435, Table 11-1) of conventional & well-known thickness for use as a conductor of electricity that have low resistivity (page 435), and in order to further increase the reflection factor of the thin film (see Kitano, paragraph 8: raising reflection factor is a stated goal of the invention), respectively.

Please note that applying a known technique (Wolf's teaching for reducing the grain size and surface roughness of a thin film) to a known device ready for improvement (device of Kitano) to yield predictable results (grain size and surface roughness of thin film are reduced) is considered to be obvious (KSR International Co. v. Teleflex Inc., 550 U.S.-, 82 USPQ2d 1385).

Regarding claim 2, Kitano discloses in FIG. 3 and related text an adhesion layer (110) and a barrier layer (109) are formed, in sequence, on said substrate, with said metal film being formed on said barrier layer.

Regarding claims 3, 4 & 6, Kitano does not disclose said metal film is formed as an alloy of at least one of Ag and Al and other metal, a proportional content of said other metal being 0.001-10 percent by weight, wherein said other metal is at least one type of metal selected from a group consisting of Cu, Mg, Si, Mn, Ti, and Cr.

Wolf teaches said metal film is formed as an alloy of at least one of Ag and Al and other metal (page 435, Table 11-1, "Aluminum / 4% Copper), a proportional content of said other metal being 0.001-10 percent by weight, wherein said other metal is at least one type of metal selected from a group consisting of Cu, Mg, Si, Mn, Ti, and Cr.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Kitano with said metal film is formed as an alloy of at least one of Ag and Al and other metal, a proportional content of said other metal being 0.001-10 percent by weight, wherein said other metal is at least one type of metal selected from a group consisting of Cu, Mg, Si, Mn, Ti, and Cr as taught by Wolf, in order to improve the film's resistance to electromigration (page 435).

Regarding claim 9, Kitano discloses in FIG. 3 and related text a semiconductor light-emitting element mounting member according to claim 1 wherein said semiconductor light-emitting element mounting member is a flat submount (see FIG. 3).

Regarding claim 10, Kitano discloses in FIG. 3 and related text a semiconductor light-emitting device wherein a semiconductor light-emitting element (100) is mounted in a semiconductor light-emitting element mounting member according to claim 1.

5. **Claims 7 & 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over (JP-2003-209286) by Kitano in view of Silicon Processing for VLSI Era Volume 1 by Wolf et al as applied to claim(s) above, and further in view of (US-2004/0026708) by Chen.

Regarding claims 7 & 8, Kitano and Wolf disclose substantially the entire claimed structure, as recited in claim 1, except a thermal expansion coefficient of said substrate is 1.times.10.sup.-6/K-10.times.10.sup.-6/K and a thermal conductivity of said substrate is at least 80 W/mK.

Chen teaches in FIG. 1 and related text a thermal expansion coefficient of said substrate (50) is 1.times.10.sup.-6/K-10.times.10.sup.-6/K and a thermal conductivity of said substrate is at least 80 W/mK (50 is a silicon substrate (paragraph 9); silicon has the thermal expansion coefficient and thermal conductivity specs stated above, by applicant's admission).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the device of Kitano and Wolf with a thermal expansion coefficient of said substrate is 1.times.10.sup.-6/K-10.times.10.sup.-6/K and a thermal conductivity of said substrate is at least 80 W/mK as taught by Chen, in order to simplify the processing steps of making the device, by using conventional & well-known substrate material.

6. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over (JP-2003-209286) by Kitano in view of Silicon Processing for VLSI Era Volume 1 by Wolf et al as applied to claim(s) above, and further in view of (US-2004/0004435) by Hsu.

Regarding claim 11, Kitano and Wolf disclose substantially the entire claimed structure, as recited in claims 1 & 10, except output is at least 1 W.

Hsu teaches in FIG. 2 and related text output is at least 1 W (paragraph 9).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the device of Kitano and Wolf with output is at least 1 W as taught by Hsu, in order to use the device in an application that requires high brightness (paragraph 9).

7. **Claims 1-4, 6, 9 & 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Silicon Processing for VLSI Era Volume 1 by Wolf et al in view of (JP-2003-209286) by Kitano.

Regarding claim 1, Wolf discloses a substrate (Fig. 4-1); and a metal film formed on a surface of said substrate, formed from Ag, Al, or an alloy containing said metals (see Table 11-1); wherein the thickness of the metal film is 0.5-3 .mu.m (page 435; "thickness range of 500-1500 nm") and crystal grains of said metal or alloy forming said metal film have a particle diameter along a surface plane of said metal film is no more than 0.5 .mu.m and said surface of said metal film has a center-line average roughness Ra of no more than 0.1 .mu.m (pages 106-107 describe the vapor deposition process; bottom of page 106: smaller grains are result of lower substrate temperature; top of page 107: smaller grains are result of higher deposition rates; these are the two methods stated by applicant in his disclosure for achieving his particle diameter and roughness specs; hence, these results are **inherent** in the application of Wolf's teaching by applicant's own disclosure; NOTE: applicant states one more factor which **may** affect particle diameter and roughness specs: roughness of the substrate; however, applicant discloses that this is not a strict requirement (page 16: "**may** not be possible")).

Wolf does not disclose a semiconductor light-emitting element mounting member comprising: a metal film functioning as an electrode layer for mounting at least one of a semiconductor light-emitting element and a reflective layer for reflecting light from a semiconductor light-emitting element.

Kitano discloses in FIG. 3 and related text (machine translation of the publication has been included) a semiconductor light-emitting element mounting member comprising: a metal film (107) functioning as an electrode layer for mounting at least one of a semiconductor light-emitting element (100) and a reflective layer for reflecting light from a semiconductor light-emitting element.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Wolf with a semiconductor light-emitting element mounting member comprising: a metal film functioning as an electrode layer for mounting at least one of a semiconductor light-emitting element and a reflective layer for reflecting light from a semiconductor light-emitting element, as taught by Kitano, in order to use the device in an application which requires a semiconductor light-emitting element mounting member, and a semiconductor light-emitting element, respectively.

Please note that combining prior art elements (Wolf's teaching of thin film and Kitano's teaching of a mounting member and light-emitting element) according to known methods (mounting the device on top of a film is known, according to Kitano) to yield predictable results is considered to be obvious (KSR International Co. v. Teleflex Inc., 550 U.S.-, 82 USPQ2d 1385).

Regarding claim 2, Wolf does not disclose an adhesion layer and a barrier layer are formed, in sequence, on said substrate, with said metal film being formed on said barrier layer.

Kitano teaches in FIG. 3 and related text an adhesion layer (110) and a barrier layer (109) are formed, in sequence, on said substrate, with said metal film being formed on said barrier layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Wolf with an adhesion layer and a barrier layer are formed, in sequence, on said substrate, with said metal film being formed on said barrier layer, as taught by Kitano, in order to form a connection with good thermal conductivity (paragraph 30), and in order to more easily plate the reflecting layer on the underlying layer than directly on substrate (paragraph 22 & paragraph 30), respectively.

Regarding claims 3, 4 & 6, Wolf discloses said metal film is formed as an alloy of at least one of Ag and Al and other metal (page 435, Table 11-1, "Aluminum / 4% Copper), a proportional content of said other metal being 0.001-10 percent by weight, wherein said other metal is at least one type of metal selected from a group consisting of Cu, Mg, Si, Mn, Ti, and Cr.

Regarding claim 9, Wolf does not disclose a semiconductor light-emitting element mounting member according to claim 1 wherein said semiconductor light-emitting element mounting member is a flat submount

Kitano teaches in FIG. 3 and related text a semiconductor light-emitting element mounting member according to claim 1 wherein said semiconductor light-emitting element mounting member is a flat submount (see FIG. 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Wolf with a semiconductor light-emitting element mounting member according to claim 1 wherein said semiconductor light-emitting element mounting member is a flat submount, as taught by Kitano, in order to use a flip chip type light-emitting element on top of it (see FIG. 3 of Kitano).

Regarding claim 10, Wolf does not disclose a semiconductor light-emitting device wherein a semiconductor light-emitting element is mounted in a semiconductor light-emitting element mounting member according to claim 1.

Kitano teaches in FIG. 3 and related text a semiconductor light-emitting device wherein a semiconductor light-emitting element (100) is mounted in a semiconductor light-emitting element mounting member according to claim 1.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Wolf with a semiconductor light-emitting device wherein a semiconductor light-emitting element is mounted in a semiconductor light-emitting element mounting member according to claim 1, as taught by Kitano, in order to use the device in an application that requires a light-emitting element.

8. **Claims 7 & 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Silicon Processing for VLSI Era Volume 1 by Wolf et al in view of (JP-2003-209286) by Kitano as applied to claim(s) above, and further in view of (US-2004/0026708) by Chen.

Regarding claims 7 & 8, Wolf and Kitano disclose substantially the entire claimed structure, as recited in claim 1, except a thermal expansion coefficient of said substrate is

1.times.10.sup.-6/K-10.times.10.sup.-6/K and a thermal conductivity of said substrate is at least 80 W/mK.

Chen teaches in FIG. 1 and related text a thermal expansion coefficient of said substrate (50) is 1.times.10.sup.-6/K-10.times.10.sup.-6/K and a thermal conductivity of said substrate is at least 80 W/mK (50 is a silicon substrate (paragraph 9); silicon has the thermal expansion coefficient and thermal conductivity specs stated above, by applicant's admission).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the device of Wolf and Kitano with a thermal expansion coefficient of said substrate is 1.times.10.sup.-6/K-10.times.10.sup.-6/K and a thermal conductivity of said substrate is at least 80 W/mK as taught by Chen, in order to simplify the processing steps of making the device, by using conventional & well-known substrate material.

9. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable Silicon Processing for VLSI Era Volume 1 by Wolf et al in view of (JP-2003-209286) by Kitano as applied to claim(s) above, and further in view of (US-2004/0004435) by Hsu.

Regarding claim 11, Wolf and Kitano disclose substantially the entire claimed structure, as recited in claims 1 & 10, except output is at least 1 W.

Hsu teaches in FIG. 2 and related text output is at least 1 W (paragraph 9).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the device of Wolf and Kitano with output is at least 1 W as taught by Hsu, in order to use the device in an application that requires high brightness (paragraph 9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Belousov whose telephone number is 571-270-3209. The examiner can normally be reached on Monday - Thursday 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander Belousov
January 4, 2008

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SUPERVISORY PATENT EXAMINER
AU 2811 TC 2800